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DESIGN AND ANALYSIS OF AN NMOS OPERATIONAL AMPLIFIER WITH DEPLETION LOADS

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The MOS transistor has become the building block for LSI digital circuits in recent years. Its small device size and high fabrication yield have made it particularly attractive.

Recently, however, the application of MOS technology to analog circuits has been studied. One particularly useful analog circuit is the operational amplifier. The ability to fabricate an all MOS operational amplifier on an LSI chip can increase the flexibility of many signal processing tasks, such as

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20. Abstract (Continued)

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In this thesis a single channel NMOS operational amplifier with depletion loads is designed. Computer simulation using the SPICE circuit analysis program is used as a design aid and to evaluate the final design, as this lends itself easily to the study of parameter variations within the circuit.

Of particular interest is the method of internal frequency compensation of the amplifier leading to design criteria for several small signal parameters. These small signal parameters are directly related to device geometry and D.C. bias conditions. Other characteristics and performance criteria of the amplifier are also discussed.

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THESIS

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1. Introduction

The MOS transistor has become the building block for LSI digital circuits in recent years. Its small device size and high fabrication yield have made it particularly attractive.

Recently, however, the application of MOS technology to analog circuits has been studied [1]. One particularly useful analog circuit is the operational amplifier. The ability to fabricate an all MOS operational amplifier on an LSI chip can increase the flexibility of many signal processing tasks, such as filtering, D/A and A/D conversion. In addition, the amplifier would be compatible with other MOS circuit elements.

In this thesis a single channel NMOS operational amplifier with depletion loads is designed. Computer simulation using the SPICE [8] circuit analysis program is used as a design aid and to evaluate the final design, as this lends itself easily to the study of parameter variations within the circuit.

Of particular interest is the method of internal frequency compensation of the amplifier leading to design criteria for several small signal parameters. These small signal parameters are directly related to device geometry and D.C. bias conditions. Other characteristics and performance criteria of the amplifier are also discussed.

2. N-Channel MOSFET Model and Parameters

2.1 Nonlinear NMOS Model

The nonlinear N-channel MOSFET model used in the design of this amplifier is shown in Figure 2.1. The subscripts D, G, S, B stand for drain, gate, source and substrate (body) respectively. It is assumed that the charge consisting of the ionized donor atoms beneath the channel is constant and that $V_{DS} \geq 0$.

The value of the current source I_D is dependent on the region of operation and is given by,

$$I_D = 0, \text{ for } V_{GS} - V_T > 0 \quad \text{(off)}$$

$$I_D = \frac{KP}{2} \frac{W}{L} [2(V_{GS} - V_T)V_{DS} - V_{DS}^2], \text{ for } 0 < V_{DS} < V_{GS} - V_T$$

$$\text{(triode region)}$$

$$I_D = \frac{KP}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}), \text{ for } 0 < V_{GS} - V_T < V_{DS}$$

$$\text{(saturation region)}$$

The various parameters in these equations are listed below. A more detailed explanation may be found in [6], [9].

W and L are the channel width and length respectively. V_T is the effective threshold voltage and is given by,

$$V_T = V_{TO} + \gamma [\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}]$$

where V_{TO} = zero substrate bias threshold voltage

γ = bulk threshold parameter

ϕ_f = fermi level of the p-substrate.

λ is the channel length modulation parameter. It is included to model the finite output conductance of the MOSFET in the saturation region. It is
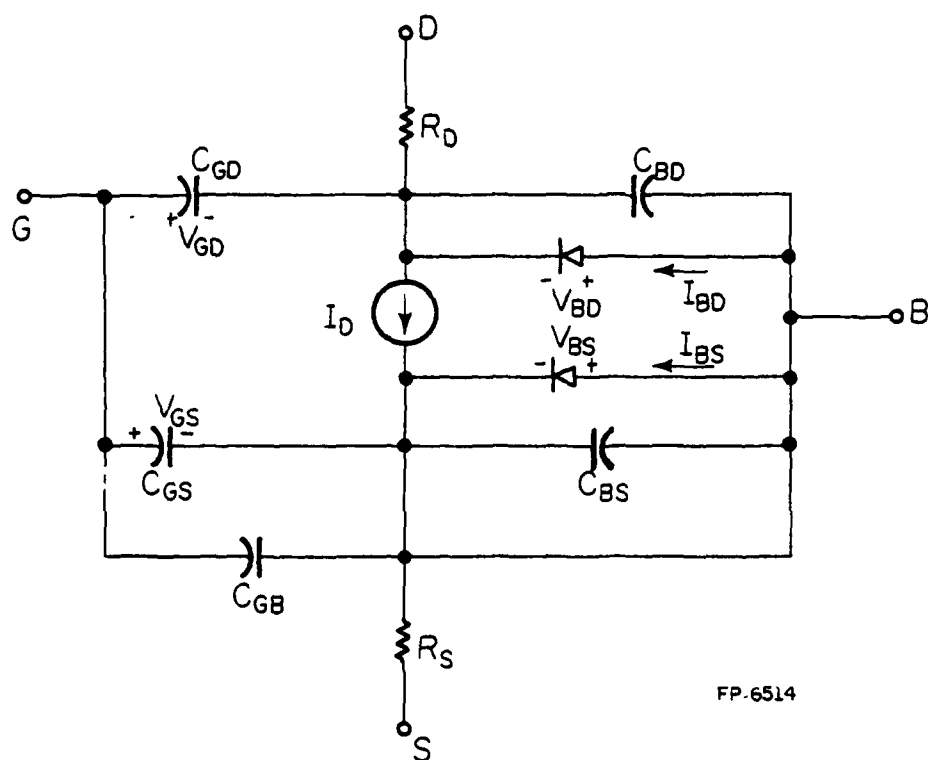
Figure 2.1 N-Channel MOSFET Nonlinear Model

given by the expression,

$$\lambda = \frac{1}{LV_{DS}} \sqrt{\frac{2\epsilon_o \epsilon_{si}}{q \, N_{SUB}} [V_{DS} - (V_{GS} - V_T)]}$$

KP is the intrinsic transconductance parameter and is given by,

$$KP = \mu_n \frac{\epsilon_o \epsilon_{ox}}{t_{ox}}$$

where μ_n and t_{ox} are the effective electron mobility and gate oxide thickness respectively.

A substrate doping of 5×10^{14} cm^{-3} and a gate oxide thickness of 1000 $\overset{o}{A}$ are used for calculations. It was also assumed that ion implantation would properly adjust V_{TO} of both depletion and enhancement devices.

Under these assumptions the following numerical values were used for the MOSFET parameters.

$$V_{TO} = \begin{cases} 0 \text{ VOLT} & \text{ENHANCEMENT} \\ -3 \text{ VOLT} & \text{DEPLETION} \end{cases}$$

$$\gamma = 0.37 \, V^{1/2}$$

$$2\phi_f = .546 \, V$$

$$KP = 20 \, \mu A/V^2$$

$$\lambda = \frac{1.63}{LV_{DS}} \sqrt{V_{DS} - (V_{GS} - V_T)} \quad \text{VOLTS}^{-1} \quad \text{(L given in } \mu m)$$

The capacitors C_{GS}, C_{GD} and C_{GB} in the MOSFET model contain voltage dependent components and therefore their values depend on the region of operation [10]. It will be assumed that all devices are operating in the saturation region, so that the following capacitances are obtained.

$$C_{GS} = \frac{2}{3} C_{OX} \times W \times L + G_{GS_o} \times W$$

$$C_{GD} = C_{GD_o} \times W$$

$$C_{GB} = 0$$

C_{OX} is the gate oxide capacitance per unit area and is given by

$$C_{OX} = \frac{\epsilon_o \epsilon_{ox}}{t_{ox}}$$

and has a numerical value of 35.4 pF/cm^2.

C_{GS_o} and C_{GD_o} are the parasitic gate to source and gate to drain

overlap capacitances per unit channel width. They are a result of the

overlap between the thin gate oxide and the n$^+$ source and drain diffusions.

The amount of overlap is process dependent. In the silicon gate process

the overlap is a result of the lateral diffusion of the source and drain

regions and is assumed to be 1 μm. This value gives,

$$C_{GS_o} = C_{GD_o} = 3.54 \text{ pF/cm}$$

The gate to substrate capacitance in the saturation region consists

of the constant gate bulk overlap capacitance. This capacitance is small

and will be ignored. This is justified by the fact that C_{GB} would always

add directly to C_{GS} or C_{GD} depending on the circuit configuration.

C_{BD} and C_{BS} are the junction capacitances of the drain and source

diffusions respectively and are voltage dependent. A reverse biased step

junction approximation will be used so that the junction capacitances per

unit junction area are given by,

$$\frac{C_{BD}}{A_D} = C_{BDO} \left[1 + \frac{V_{DB}}{\phi_B} \right]^{-1/2}$$

$$\frac{C_{BS}}{A_S} = C_{BSO} \left[1 + \frac{V_{SB}}{\phi_B} \right]^{-1/2}$$

where C_{BDO} and C_{BSO} are the zero bias values of C_{BD} and C_{BS} and ϕ_B is the junction potential, assumed to be 0.8 volt. Calculations yield

$$C_{BDO} = C_{BSO} = 7.3 \ \eta F/cm^2$$

A_D is the junction area associated with the drain diffusion while to a first order approximation A_S is the junction area associated with the source diffusion plus the area of the depletion region under the channel. These relations are expressed as,

$$A_D = A_{D_{DIFF.}} \qquad A_S = A_{S_{DIFF.}} + W \times L$$

The area terms $A_{D_{DIFF.}}$ and $A_{S_{DIFF.}}$ are a function of the layout rules which would be used if the circuit were actually realized. The minimum layout rules assumed in the design are: 1) The minimum distance between metalization is 8 μm. 2) The minimum contact holes size is 10 μm $\times$ 10 μm. 3) The minimum metal overlap around a contact hole is 2.5 μm. 4) The minimum n^+ margin around the contact is 5 μm. A more detailed discussion of layout rules is given in [6]. Using these rules the terms A_D and A_S were approximated.

Since the substrate is always kept at the lowest potential in the circuit the source and drain junctions are always reverse biased. Therefore the saturation currents I_{BD} and I_{BS} are negligibly small and may be ignored.

R_D and R_S, representing the ohmic contact resistance, are nominally 50 ohms and may also be ignored since they have little effect on circuit operation.

2.2 Small Signal NMOS Model

It will be assumed in this thesis that the MOSFET will always be biased in the saturation region. By linearizing the expression for I_{DS} with respect

to V_{GS}, V_{DS} and V_{BS} we obtain

$$i_d = g_m v_{gs} + g_d v_{ds} + g_{mb} v_{bs}$$

where g_m = transconductance = $\left. \dfrac{\partial I_{DS}}{\partial V_{GS}} \right|_{V_{DS}, \ V_{BS}}$

$\quad g_d$ = output conductance = $\left. \dfrac{\partial I_{DS}}{\partial V_{DS}} \right|_{V_{GS}, \ V_{BS}}$

$\quad g_{mb}$ = bulk transconductance = $\left. \dfrac{\partial I_{DS}}{\partial V_{BS}} \right|_{V_{GS}, \ V_{DS}}$

The lower case letters represent AC quantities. This results in the small signal NMOS model in Figure 2.2.

Performing the partial differentiation while assuming λ is a constant parameter we obtain,

$$g_m = KP \frac{W}{L} (V_{GS} - V_T)(1 + \lambda V_{DS}) = \frac{2 I_D}{(V_{GS} - V_T)}$$

$$g_d = \frac{KP}{2} \frac{W}{L} (V_{GS} - V_T)^2 \lambda = I_D \left(\frac{\lambda}{1 + \lambda V_{DS}} \right)$$

$$g_{mb} = KP \frac{W}{L} (V_{GS} - V_T)(1 + \lambda V_{DS}) \frac{\gamma}{2} (V_{SB} + 2\phi_f)^{-1/2}$$

$$= \frac{g_m \gamma}{2(V_{SB} + 2\phi_f)^{1/2}}$$

It should be observed that these small signal parameters are closely related to bias conditions and are all directly proportional to I_D.
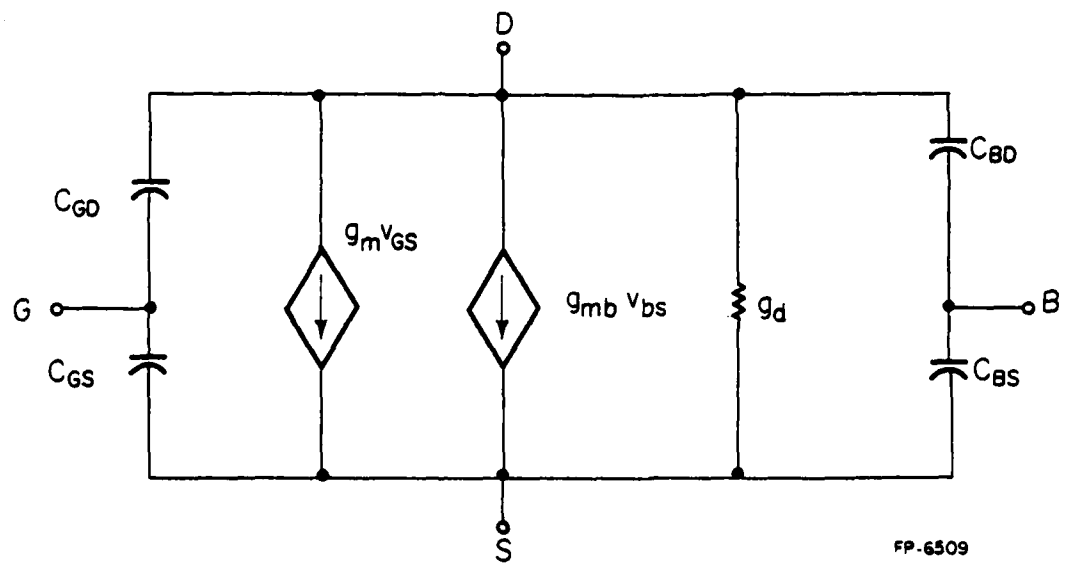
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Figure 2.2   Small Signal NMOS Model

3. Depletion vs. Enhancement MOSFETS as Active Loads

In order to minimize circuit area, MOSFETS operating in the saturation region are used as loads. In single channel technology there are two commonly used load configurations.

The first configuration uses an enhancement MOSFET ($V_T > 0$ for n-channel) with gate tied to drain. This is illustrated in the common source stage in Figure 3.1a. Since V_{GS} is equal to V_{DS} the load device is in saturation as long as the source is at a potential V_T volts below the drain. Replacing the load device with its small signal model the effective load resistance is

$$R_{L_{ENH.}} = \frac{1}{g_{m_2} + g_{mb_2} + g_{d_2}} \; .$$

as shown in Figure 3.1b. It is generally the case that $g_m > g_{mb} > g_d$.

The second configuration uses a depletion MOSFET ($V_T < 0$ for n-channel) with gate tied to source. A common source stage utilizing a depletion load is shown in Figure 3.2a. Since $V_{GS} = 0$ a negative threshold voltage is essential for current flow. The load device will remain in the saturation region as long as the source is at a potential $|V_T|$ volts below the drain. Again, replacing the load with its small signal model the effective load resistance for the depletion device is

$$R_{L_{DEP.}} = \frac{1}{g_{mb_2} + g_{d_2}}$$

as shown in Figure 3.2b.

Comparing the small signal load resistances in both cases we see that $R_{L_{DEP.}} > R_{L_{ENH.}}$ due to the absence of the g_{m_2} term in the expression for $R_{L_{DEP.}}$. The absence of the g_{m_2} is a result of fixing $V_{GS} = 0$ by connecting
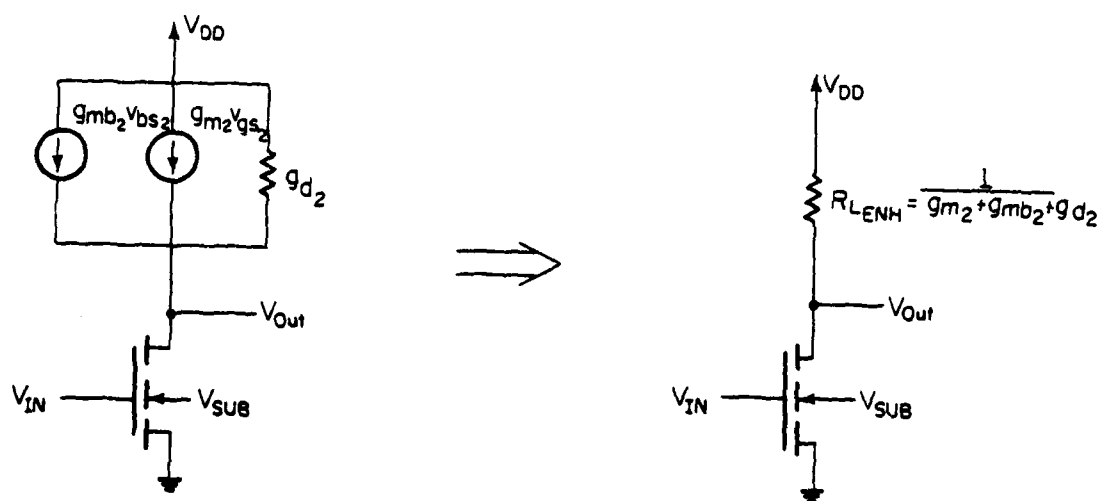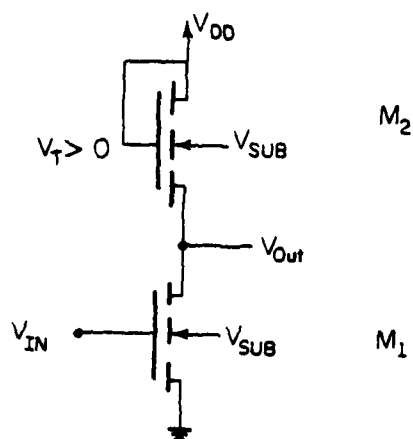
Figure 3.1   Common Source Stage With Enhancement Load
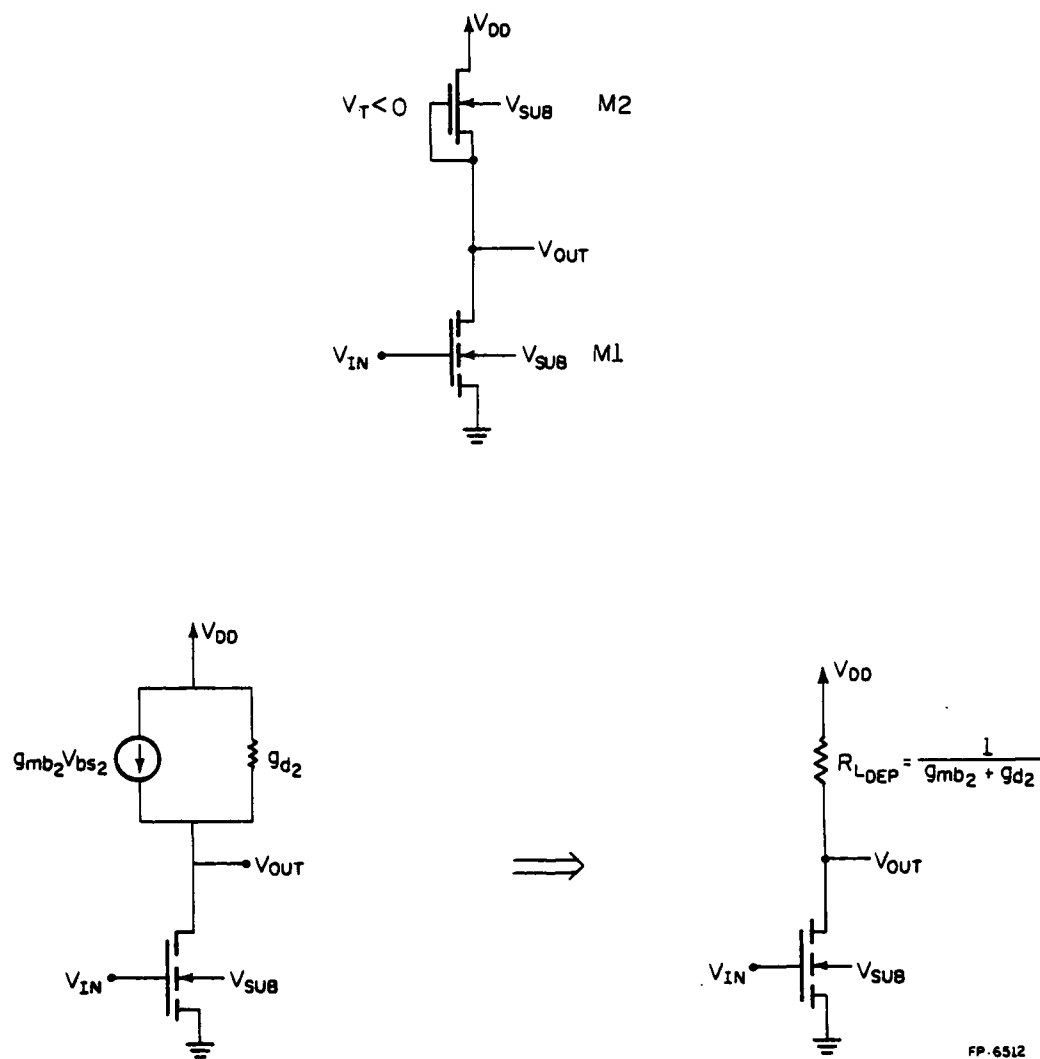
Figure 3.2   Common Source Stage With Depletion Load

the gate and source terminals. Since g_m is usually 4 to 5 times larger than $g_{mb} + g_d$, the voltage gain of the common source stage, given by $A_v = g_{m_1} R_L$, can be significantly increased by using depletion rather than enhancement loads.

4. Design of the Amplifier

The actual design of the amplifier was subject to several design objectives. The first goal was to obtain an open loop voltage gain of 1000 and a unity gain bandwidth greater than 2 MHz. A wide common mode range for the differential input and a common mode rejection ratio of at least 60 db was also desired. Most important was the requirement that the amplifier remain stable in closed loop feedback configurations and be able to drive small capacitive loads up to 20 pF.

Figure 4.1 shows the complete schematic for the amplifier. Although not shown in Figure 4.1, the substrate terminal of each MOSFET is tied to -2.5 volts. V_{DD} was chosen to be +15 volts. The geometry, operating point, and small signal parameters for each device are listed in Table 4.1.

The amplifier is divided into three sections consisting of the differential/level shift, cascode and output stages. The design of each stage will be considered separately in the following sections.
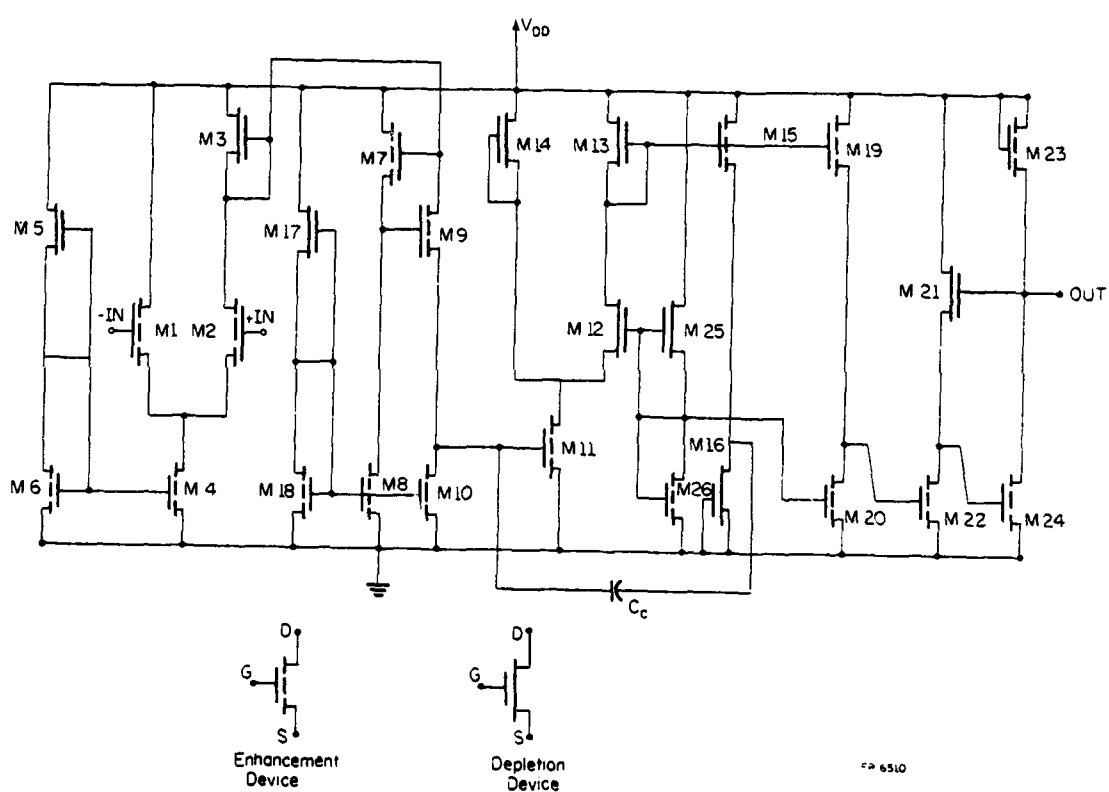
Figure 4.1 Amplifier Schematic

Table 4.1 MOSFET Operating Points and Small Signal Parameters

Device	Channel Dimensions	(μm)	Type	Capacitances (pF)			
	W	L		C_{GS}	C_{GD}	C_{BS}	C_{BD}
M1	250	15	E	0.952	0.089	0.107	0.002
M2	250	15	E	0.952	0.089	0.107	0.040
M3	20	27.5	D	0.134	0.007	0.399	0.002
M4	70	161	E	2.620	0.025	0.004	0.105
M5	16	40	D	0.153	0.006	0.013	0.002
M6	7	21	E	0.036	0.002	0.004	0.016
M7	10	130	E	0.303	0.004	0.028	0.002
M8	40	20	E	0.198	0.014	0.004	0.028
M9	250	15	E	0.952	0.089	0.094	0.056
M10	17	20	E	0.084	0.006	0.004	0.094
M11	112	15	E	0.426	0.040	0.004	0.026
M12	150	20	D	0.744	0.053	0.077	0.027
M13	27.2	20	D	0.135	0.010	0.035	0.002
M14	80	20	D	0.397	0.028	0.077	0.002
M15	30	20	E	0.149	0.011	0.012	0.002
M16	20	20	D	0.099	0.007	0.004	0.012
M17	14.5	40	D	0.139	0.005	0.015	0.002
M18	30.5	20	E	0.151	0.001	0.004	0.018
M19	10	115	E	0.268	0.004	0.030	0.002
M20	65	20	E	0.322	0.023	0.004	0.030
M21	17	100	D	0.397	0.006	0.049	0.002
M22	39	20	E	0.193	0.014	0.004	0.016
M23	15	20	E	0.074	0.005	0.022	0.002
M24	76	20	E	0.377	0.027	0.002	0.022
M25	14.5	40	D	0.139	0.005	0.015	0.002
M26	30.5	20	E	0.151	0.011	0.004	0.018

Table 4.1 MOSFET Operating Points and Small Signal Parameters
(continued)

Device	Device Current		Operating Point (V)		Conductances (μU)		
	I_D (μA)	V_{GS}	V_{DS}	V_{BS}	g_m	g_d	g_{mb}
M1	15.4	1.13	8.63	- 8.87	114	6.24	6.85
M2	13.2	1.13	4.47	- 8.87	97.9	0.46	5.86
M3	27.2	0.0	4.17	-13.30	28.7	5.93	1.38
M4	28.6	3.03	6.38	- 2.50	21.6	0.088	1.96
M5	23.7	0.0	11.97	- 5.53	20.1	0.27	1.39
M6	23.7	3.03	3.03	- 2.50	17.9	0.78	1.62
M7	34.2	7.42	11.60	- 5.91	10.2	0.11	0.61
M8	34.2	1.65	3.41	- 2.50	53.8	1.58	5.24
M9	14.0	0.85	8.27	- 5.06	114	0.84	8.80
M10	14.0	1.65	2.56	- 2.50	22	0.62	2.14
M11	374	2.56	3.21	- 2.50	343	17.2	31.8
M12	55.3	-1.56	7.18	- 5.71	140	2.11	10.1
M13	55.3	0.0	4.62	-12.88	57.7	1.93	2.82
M14	319	0.0	11.79	- 5.71	272	14.8	18.6
M15	89.4	3.01	7.63	- 9.87	85.6	5.15	4.69
M16	89.4	0.0	7.37	- 2.50	68.3	5.07	6.19
M17	23.7	0.0	13.35	- 4.15	19.2	0.27	1.48
M18	23.7	1.65	1.65	- 2.50	37.3	0.75	3.63
M19	52.8	8.10	12.72	- 4.78	14.1	0.61	0.90
M20	52.8	1.65	2.28	- 2.5	83.0	2.32	8.09
M21	73.5	4.30	11.96	- 5.54	22.1	0.29	1.37
M22	73.5	2.28	3.04	- 2.5	77.4	3.35	7.28
M23	350	7.66	7.66	- 9.85	104	3.79	5.26
M24	350	3.04	7.35	- 2.5	263	19.8	23.8
M25	23.7	0.0	13.35	- 4.15	19.2	0.27	1.48
M26	23.7	1.65	1.65	- 2.50	37.3	0.75	3.63

4.1 Differential/Level Shift Section

The first section of the amplifier consists of a differential input stage followed by a level shift stage. The differential stage is single ended consisting of the differential pair M1 and M2 driving the load M3. The current source M4 is biased by the voltage divider M5 and M6. A level shifting stage consisting of M7, M8, M9 and M10 follows the differential stage and shifts the DC level from 10.84 volts down to 2.56 volts. Another voltage divider consisting of M17 and M18 biases the loads M8 and M10.

The expression for the differential gain from the inputs to the source of M3 is given by,

$$A_d = 1/2 \; \frac{\left[\left(g_1 + g_{d_4}\right)g_{m_2} + g_{m_1}g_2\right]}{\left(g_{d_3} + g_{mb_3} + \alpha g_{d_{10}}\right)\left(g_1 + g_2 + g_{d_4}\right) + g_{d_2}\left(g_1 + g_{d_4}\right)}$$

where α is the gain of the level shift stage and

$$g_k = g_{m_k} + g_{d_k} + g_{mb_k} \qquad k = 1, 2, \ldots$$

The $\alpha g_{d_{10}}$ term in the denominator represents the additional load conductance presented by the level shift stage.

The gain of the level shift stage is given by,

$$\alpha = \frac{g_{m_7}g_{m_9} + g_{d_9}\left(g_7 + g_{d_8}\right)}{\left(g_7 + g_{d_8}\right)\left(g_9 + g_{d_{10}}\right)}$$

which is always less the unity. The common mode gain of the differential stage may be approximated by,

$$A_c \simeq \frac{1}{2} \cdot \frac{g_{d_4}}{g_{d_3} + g_{mb_3} + \alpha g_{d_{10}}}$$

Therefore, to achieve a low common mode gain, g_{d_4} should be minimized by

making M4 a long channel device.

Substituting numerical values for the small signal parameters yields a differential gain of 19.6 and a level shift gain of 0.755. The common mode gain is 0.018 when evaluated using the above equation whereas computer simulation gives a value of 0.015. The common mode rejection ratio may now by computed as,

$$CMRR = \frac{A_d}{A_c} = 62.3 \text{ db}$$

which satisfies the design goal.

The combined differential/level shift section was found to have a combined gain of 23.4 db when a differential input was applied and 3 db bandwidth of 1 MHz. The output impedance at the drain of M10 was found to be 287 kohms.

The common mode range of the inputs is determined by the voltages V9 and V4 in Figure 4.2. The upper limit for the common mode voltage, VCOM, occurs when VCOM-V9 equals the threshold voltage of M2. Any further increase in VCOM would result in M2 entering the triode region. The lower limit for VCOM occurs when VCOM-V4 equals the threshold voltage of M1 and M2. If VCOM is lowered further M1 and M2 will become cut off.

To achieve an acceptable upper limit for VCOM a modified level shift stage with feedback element M9 was designed rather than using a single source follower stage. The level shift stage effectively maintains V9 at its quiescent value by maintaining a constant current through M3. The operation may be explained as follows. Increasing VCOM from its nominal value of 7.5 volts results in an increase in currents I1 and I2 due to the increase in V4 (Recall $I_4 \propto (1 + \lambda V_{D4})$). An increase in I2 also means an increase in I_3 which in this case is given by,

$$I_3 = I_9 + I_2$$
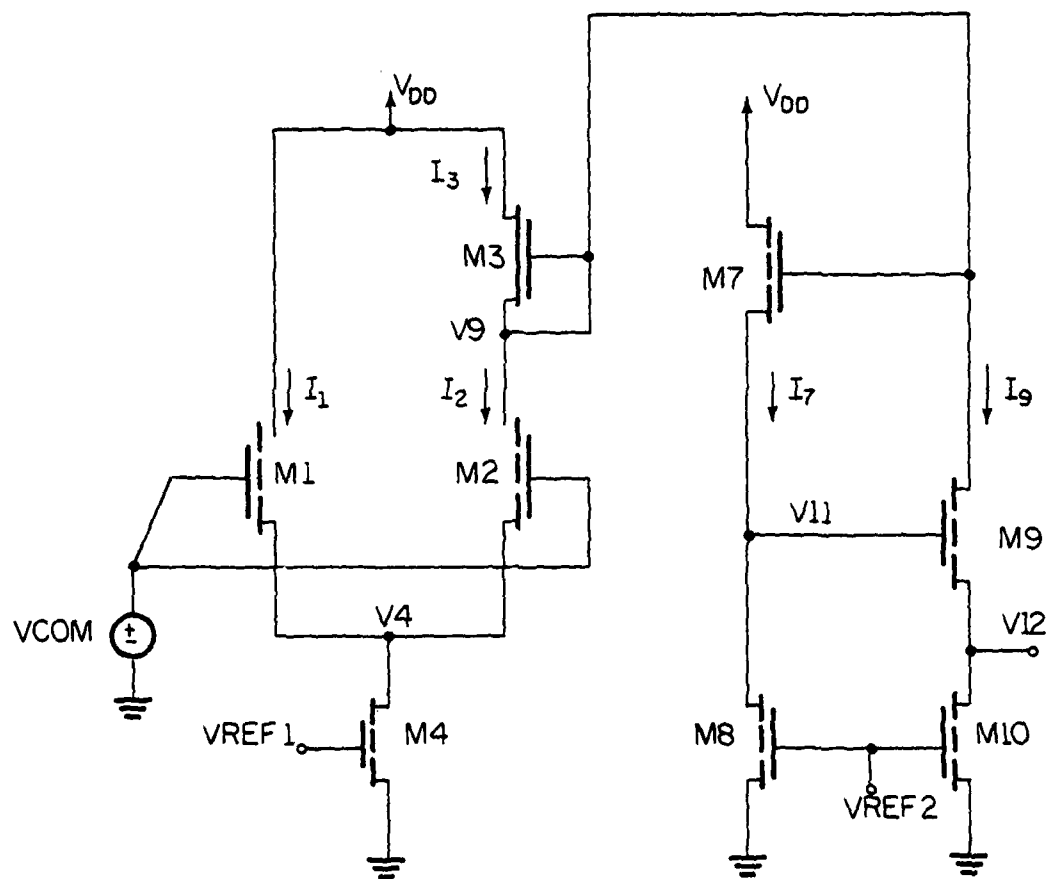
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Figure 4.2 Differential/Level Shift Stage

$$I3 = \frac{KP}{2}\left(\frac{W}{L}\right)_3 [3 - .37 (\sqrt{15 - V_{DS_3} + 2\phi_f} - \sqrt{2\phi_f})]^2 [1 + \lambda_3 V_{DS_3}]$$

Thus if I3 is increased, V_{DS_3} will also increase lowering the upper limit for VCOM.

Because M7 has a long narrow channel its gate to source voltage is large and remains fixed for a constant current I7. Thus if V9 should start to decrease, due to an increase in I3, V11 will drop by the same amount. The drop in V11, however, will decrease I9 and consequently I3. The decrease in I3 will decrease V_{DS3}, moving V9 back up to its quiescent value.

It should be noted that variations in I3 due to changes in VCOM can be minimized initially by designing M4 to have a long channel. A similar level shift stage has been reported previously [2] which besides insuring a large common mode range also allows a wide variation in supply voltage by using a balanced level shift stage which requires more transistors.

Computer simulation shows that a common mode variation of $\pm$ 4 volts from the designed value of VCOM = 7.5 volts results in only a 1.1% change in the quiescent voltage V9.

4.2 Cascode Stage

The second section of the amplifier is a cascode stage consisting of M11, M12, M13 and M14. The effective load resistance of M13 is $(g_{mb_{13}} + g_{d_{13}})^{-1}$ which is inversely proportional to its quiescent current I13. Device M12, operated in a common gate configuration, decreases the Miller capacitance associated with the driving device M11 thereby increasing the bandwidth of this stage. Device M12 is biased by the voltage divider consisting of M25 and M26. M14 acts as a constant current source which increases the trans-conductance of M11 by increasing its quiescent current.

The voltage gain of a cascode stage without the current source M14 is given by,

$$A = \frac{-g_{m_{11}} g_{12}}{(g_{mb_{13}} + g_{d_{13}})(g_{12} + g_{d_{11}}) + g_{d_{11}} g_{12}} \simeq \frac{-g_{m_{11}}}{(g_{mb_{13}} + g_{d_{13}})}$$

The approximation to A is valid when the output conductances of M11 and M12 are small compared to g_{12}. The voltage gain with the current source M14 present is given by,

$$A' = \frac{-g'_{m_{11}} g_{12}}{(g_{mb_{13}} + g_{d_{13}})(g_{12} + g'_{d_{11}} + g_{d_{14}} + g_{mb_{14}}) + (g'_{d_{11}} + g_{d_{14}} + g_{mb_{14}}) g_{d_{12}}}$$

which is similar to the expression for A except that the $g_{d_{11}}$ term has been replaced by $g'_{d_{11}} + g_{d_{14}} + g_{mb_{14}}$. Again if g_{12} is much larger than $g'_{d_{11}} + g_{d_{14}} + g_{mb_{14}}$ and the product term $(g'_{d_{11}} + g_{d_{14}} + g_{mb_{14}}) g_{d_{12}}$ is negligible the gain may be approximated by,

$$A' \simeq \frac{-g'_{m_{11}}}{(g_{mb_{13}} + g_{d_{13}})}$$

where $g'_{m_{11}} > g_{m_{11}}$ due to the additional current flowing through M11. A

significant voltage gain may therefore be achieved by increasing the ratio

I_{14}/I_{13}.

Substituting numerical values into the expression for A' results in

a value of -48.9. The stage is also found to be fairly broadband having

a 3 db bandwidth of 3.9 MHz. A more detailed description of the frequency

characteristics of this stage will be considered in the chapter on

frequency compensation.

4.3 Output Stage

An output stage with a wide bandwidth and low output impedance is desired to minimize loading effects when driving capacitive loads. Also, the quiescent current of the output stage should be large enough to ensure a fast enough rise time under transient conditions.

The output stage in the final design consists of devices M19 through M24. M19 and M20 form a source follower which shifts the DC voltage at the output of the cascode stage from 10.38 volts to 2.28 volts. Devices M21, M22, M23 and M24 form two common source stages employing local feedback through device M21.

This configuration is widely used in single channel tε ₁nology [2], [3], [5] due to the lack of complimentary devices. A source follower stage which can achieve low output impedance has been used [4] but its usefulness as an output stage is limited by its restricted voltage swing. A common source stage has a wider output swing but a very large quiescent current is required to gain an acceptable value of output impedance. The feedback configuration under consideration has an acceptable output swing while achieving a low output impedance through feedback.

The voltage gain of the output stage without feedback is given by,

$$A = \frac{\alpha g_{m_{22}} g_{m_{24}}}{(g_{21} + g_{d_{22}})(g_{23} + g_{d_{24}})}$$

where α is the gain of the source follower stage.

The output impedance is approximately the load resistance of M23 and is given by,

$$R_o = \frac{1}{g_{23} + g_{d_{24}}} .$$

When the feedback is connected the expression for the voltage gain changes to,

$$A_f = \frac{\alpha g_{m_{22}} g_{m_{24}}}{(g_{21} + g_{d_{22}})(g_{23} + g_{d_{24}}) + g_{m_{24}} g_{m_{21}}} = \frac{A}{1 + BA}$$

where $B = \dfrac{g_{m_{21}}}{g_{m_{22}}}$.

The output impedance is also reduced by the same factor and is given by,

$$R_{o_f} = \frac{g_{21} + g_{d_{22}}}{(g_{21} + g_{d_{22}})(g_{23} + g_{d_{24}}) + g_{m_{24}} g_{m_{21}}}$$

Substituting numerical values from Table 4.1 into the previous equations gives a gain of 1.7 and an output impedance of 2.87 kohms. The 3 db bandwidth is found to be 6 MHz which satisfies the requirement that it be a broadband stage.

5. Frequency Compensation

Because the amplifier must remain stable when used in unity gain feedback configurations it is necessary that its gain fall below unity before its phase exceeds 180 degrees. Figure 5.1 shows the gain and phase curves of the uncompensated amplifier. The above requirement has not been met since the phase reaches 180 degrees at 2.5 MHz while unity gain doesn't occur until 13 MHz.

To remedy the situation, a dominant pole is created at approximately 1.5 kHz. This creates a 20 db per decade rolloff in gain while degrading the phase by only 90 degrees. When the frequency corresponding to the uncompensated poles is reached the gain will be below unity and further decreases in phase will be of no consequence.

To create the dominant pole a feedback capacitor C_c, is placed around an inverting stage as shown in Figure 5.2 where R_s represents the output resistance of the previous stage. Assuming a constant gain of A_o, the transfer function V_o/V_s may be computed as,

$$\frac{V_o}{V_s} = \frac{-A_o}{1 + SR_s C_c (A_o + 1)}$$

which for the case when $A_o \gg 1$ may be reduced to,

$$\frac{V_o}{V_s} = \frac{-A_o}{1 + SR_s A_o C_c} \, .$$

Notice that the compensation capacitor has been effectively multiplied by A_o which allows a physically small, on chip capacitor to create a dominant low frequency pole at

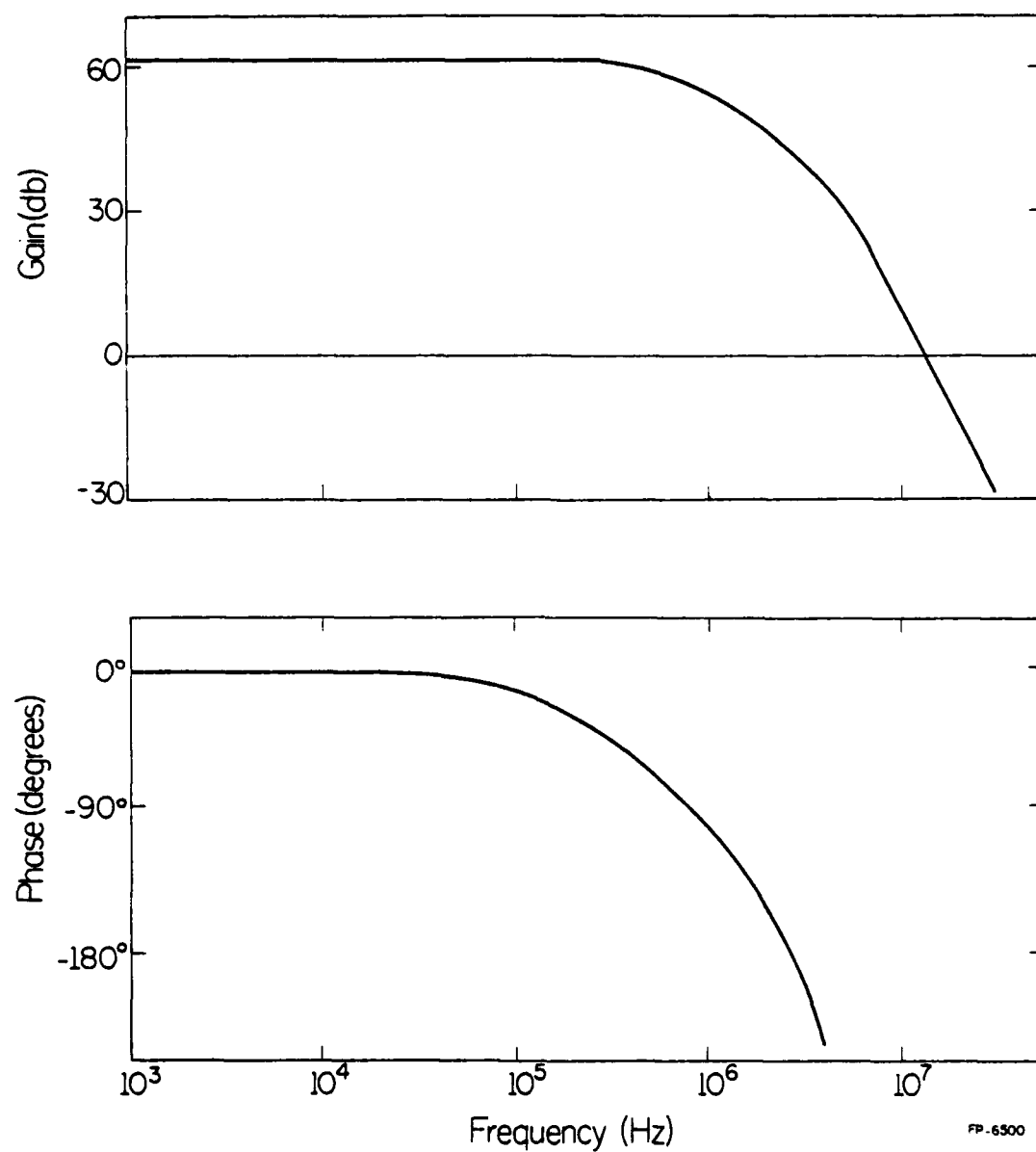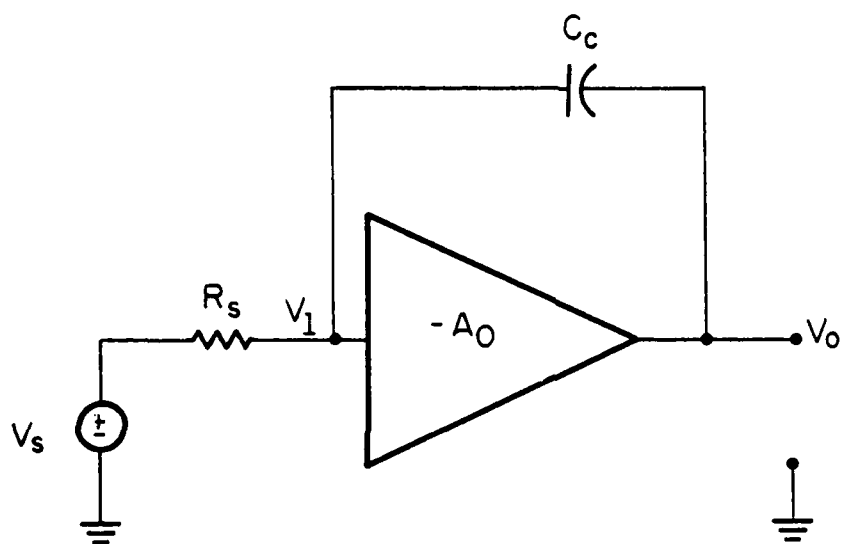$$\omega_d = \frac{1}{R_s C_c A_o}$$

Figure 5.1 Uncompensated Frequency Response

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Figure 5.2   Capacitive Feedback Scheme

It is well known [7] however that the configuration in Figure 5.2 does not lend itself to MOS circuits. The problem may be explained by replacing the ideal gain stage of Figure 5.2 with the frequency dependent cascode stage as shown in Figure 5.3a. The corresponding small signal model is shown in Figure 5.3b. Applying nodal analysis, the numerator of the transfer function V_o/V_s is found to be,

$$\text{NUM } [V_o/V_s] = S^2 + \left[\frac{(g_{12} + G_{L_{11}})}{C_2 + C_3} + \frac{g_{12}C_2}{(C_2 + C_3) C_c} \right] S - \frac{g_{m_{11}}g_{12}}{(C_2 + C_3) C_c}$$

The roots of this equation give the zeroes of the transfer function, one of which will lie in the right half of the S-plane.

To study the locations of the two zeroes a root locus diagram as a function of $g_{m_{11}}$ is provided in Figure 5.4. Other parameters were assumed to take on constant values given in Table 4.1 and C_c was assumed to be 10 pF. All values in the S-plane have been normalized by a factor of 2π so that a clearer correspondence can be made between zero locations and their effect on the gain and phase of the transfer function.

As can be seen the right half plane (RHP) zero starts at the origin and moves to the right as $g_{m_{11}}$ increases. If the RHP zero is too close to the origin the frequency compensation scheme is upset in two ways: 1) The 20 db per decade rolloff initiated by the dominant pole is prevented. 2) The phase is degraded by an additional 90 degrees which causes the 180 degrees phase crossing to occur at a lower frequency. Figure 5.5 illustrates the effects of a low frequency RHP zero on the gain and phase of a typical three-pole compensated amplifier.
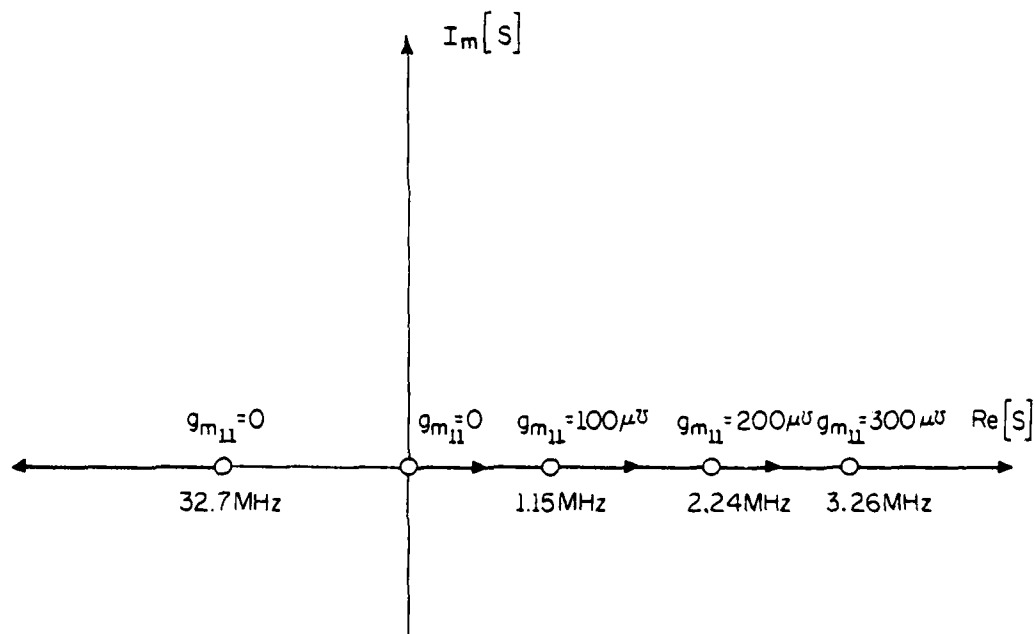
Clearly the RHP zero must be pushed to the right beyond the designed unity gain frequency so that its effects are minimized. However $g_{m_{11}}$ may
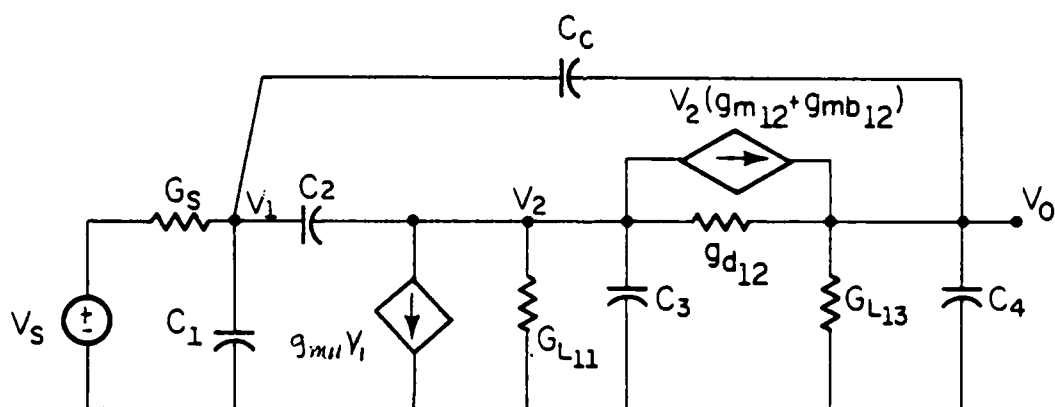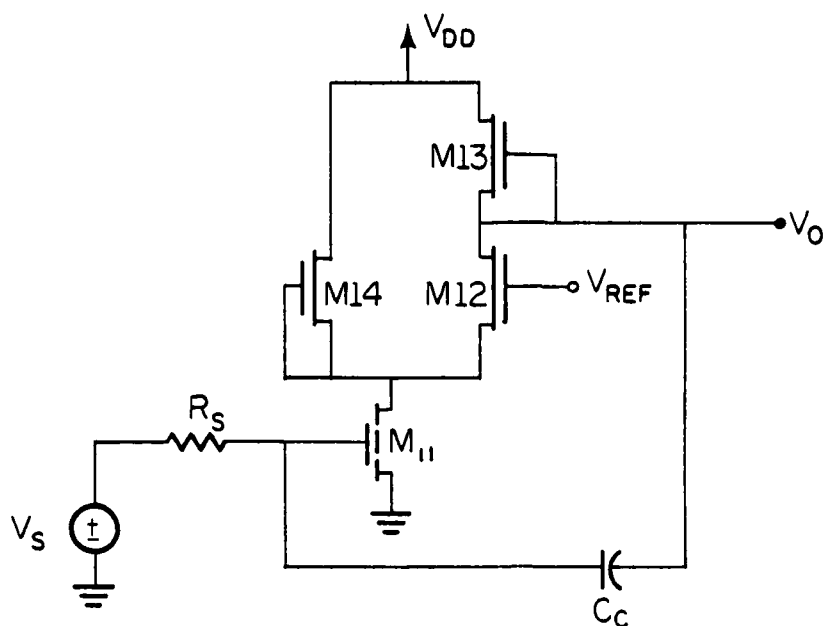
$$G_{L_{13}} = g_{d_{13}} + g_{mb_{13}}$$
$$G_{L_{11}} = g_{d_{11}} + g_{d_{14}} + g_{mb_{14}}$$
$$C_1 = C_{GS_{11}}$$
$$C_2 = C_{GD_{11}}$$
$$C_3 = C_{BD_{11}} + C_{GS_{12}} + C_{BS_{12}} + C_{BS_{14}} + C_{GD_{14}}$$

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Figure 5.3 Cascode Stage With Capacitive Feedback
a) Circuit Implementation b) Small Signal Circuit

$$G_{L_{11}} = 50.5 \mu\text{U}$$
$$g_{12} = 152.2 \mu\text{U}$$
$$C_{12} = 10\text{pf}$$
$$C_c = 10\text{pf}$$
$$C_1 = .426\text{pf}$$
$$C_2 = .0396\text{pf}$$
$$C_3 = .952\text{pf}$$

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Figure 5.4   Locus of Zeroes as a Function of $g_{m_{11}}$
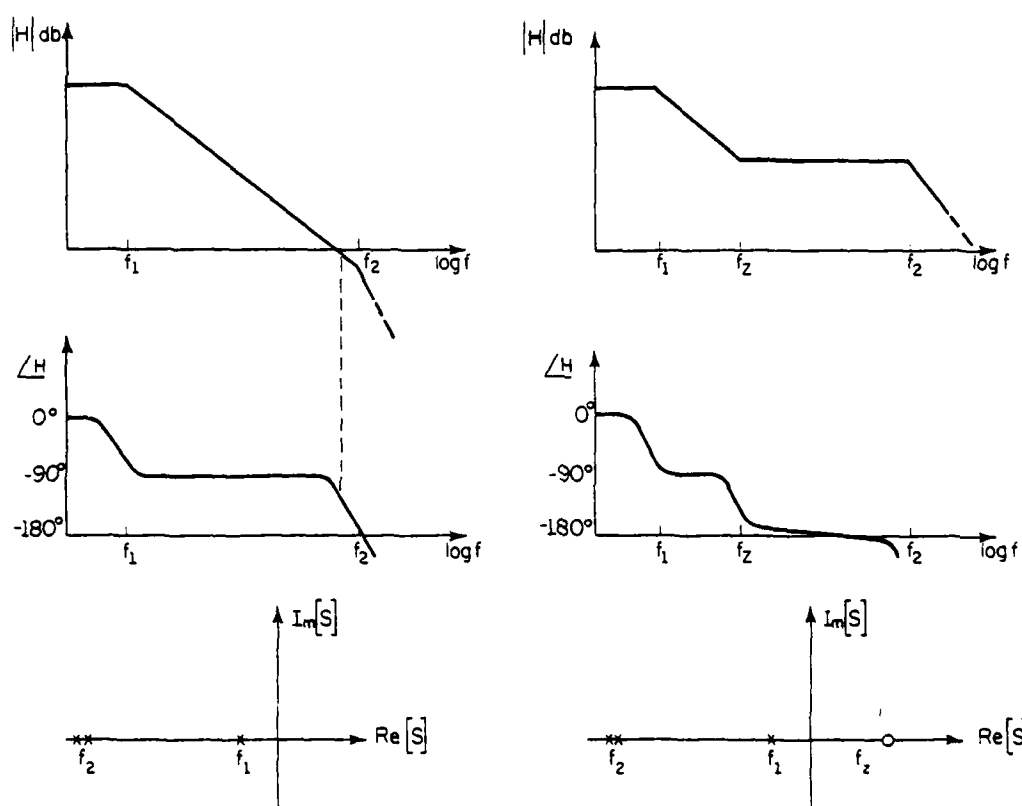
Figure 5.5 Effect of RHP Zero on Transfer Function

not be increased indefinitely due to practical considerations such as device size, parasitic capacitance and quiescent current.

Another method of moving the RHP zero to the right is illustrated in Figure 5.6 where a root locus diagram for the same numerator as a function of C_c is constructed. It is seen that decreasing C_c has the same effect on the RHP zero as increasing $g_{m_{11}}$. Decreasing C_c however will move the dominant pole to a higher frequency again upsetting the compensation scheme.

To get around this problem a buffer amplifier consisting of transistors M15 and M16 in Figure 4.1 is inserted in the capacitive feedback loop. It will be shown that the buffer amplifier prevents signal feedforward which is equivalent to reducing C_c in regard to the numerator of V_o/V_s while the dominant pole remains unchanged.

The new configuration is shown in Figure 5.7 with a source follower stage acting as the buffer amplifier. The small signal equivalent circuit is also shown. The frequency of the dominant pole is now given by,

$$\omega_d = \frac{1}{R_s C_c A_o A_f}$$

and is affected very little by the buffer amplifier since $A_f \simeq 1$. Applying nodal analysis to Figure 5.7c results in a new expression for the numerator of V_o/V_s,

$$\text{NUM}\left[\frac{V_o}{V_s}\right] = s^3 + s^2 \left[\frac{g_{12} + G_{L_{11}}}{C_2 + C_3} + \frac{g_{12}C_2(C_c + C_6 + C_7)}{(C_2 + C_3)\,C_6 C_c}\right] + s\left[\frac{g_{12}(G_{L_{14}} + g_{m_{15}})C_2}{(C_2 + C_3)\,C_6 C_c}\right.$$
$$\left. - \frac{g_{12}g_{m_{11}}(C_c + C_6 + C_7)}{(C_2 + C_3)\,C_6 C_c}\right] - \frac{g_{12}g_{m_{11}}(G_{L_{14}} + g_{m_{15}})}{(C_2 + C_3)\,C_6 C_c}$$
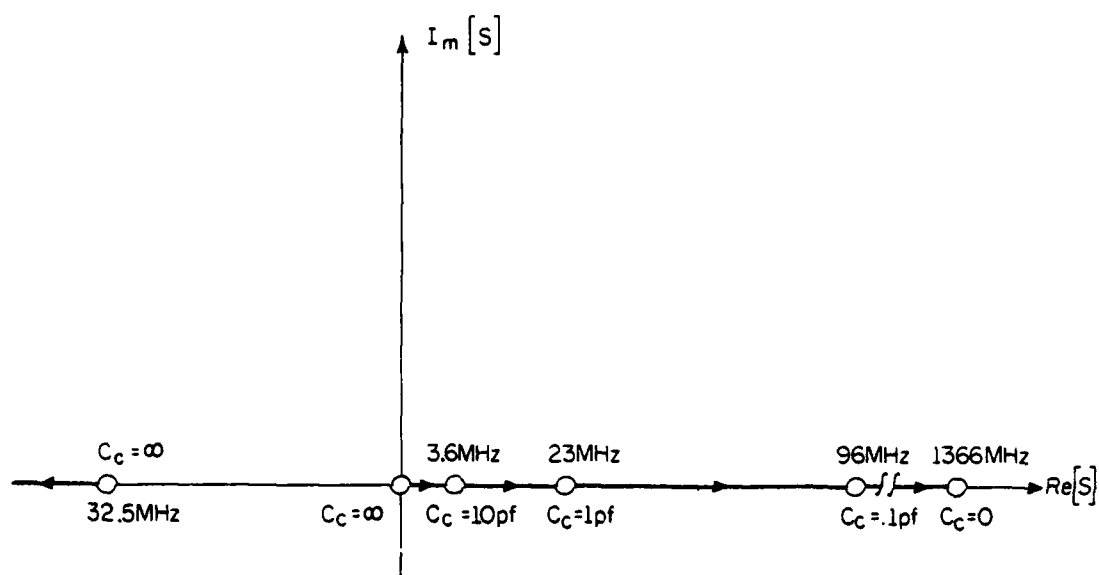
$G_{L11} = 50.5 \mu \mho$
$gm_{11} = 340 \mu \mho$
$g_{12} = 152.2 \mu \mho$
$C_1 = 0.426 pf$
$C_2 = 0.0396 pf$
$C_3 = 0.952 pf$

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Figure 5.6   Locus of Zeroes as a Function of C_c

$$G_{L_{11}} = gd_{11} + gd_{14} + gmb_{14}$$
$$G_{L_{13}} = gd_{13} + gmb_{13}$$
$$G_{L_{14}} = gd_{15} + gmb_{15} + gd_{16}$$

$$C_1 = C_{GS11}$$
$$C_2 = C_{GD11}$$
$$C_3 = C_{BD11} + C_{GS12} + C_{BS12} + C_{BS14} + C_{GD14}$$
$$C_4 = C_{BS13} + C_{GD13} + C_{BD12} + C_{GD12} + C_{GD15}$$
$$C_6 = C_{GS15}$$
$$C_7 = C_{BS15} + C_{BD16} + C_{GD16}$$
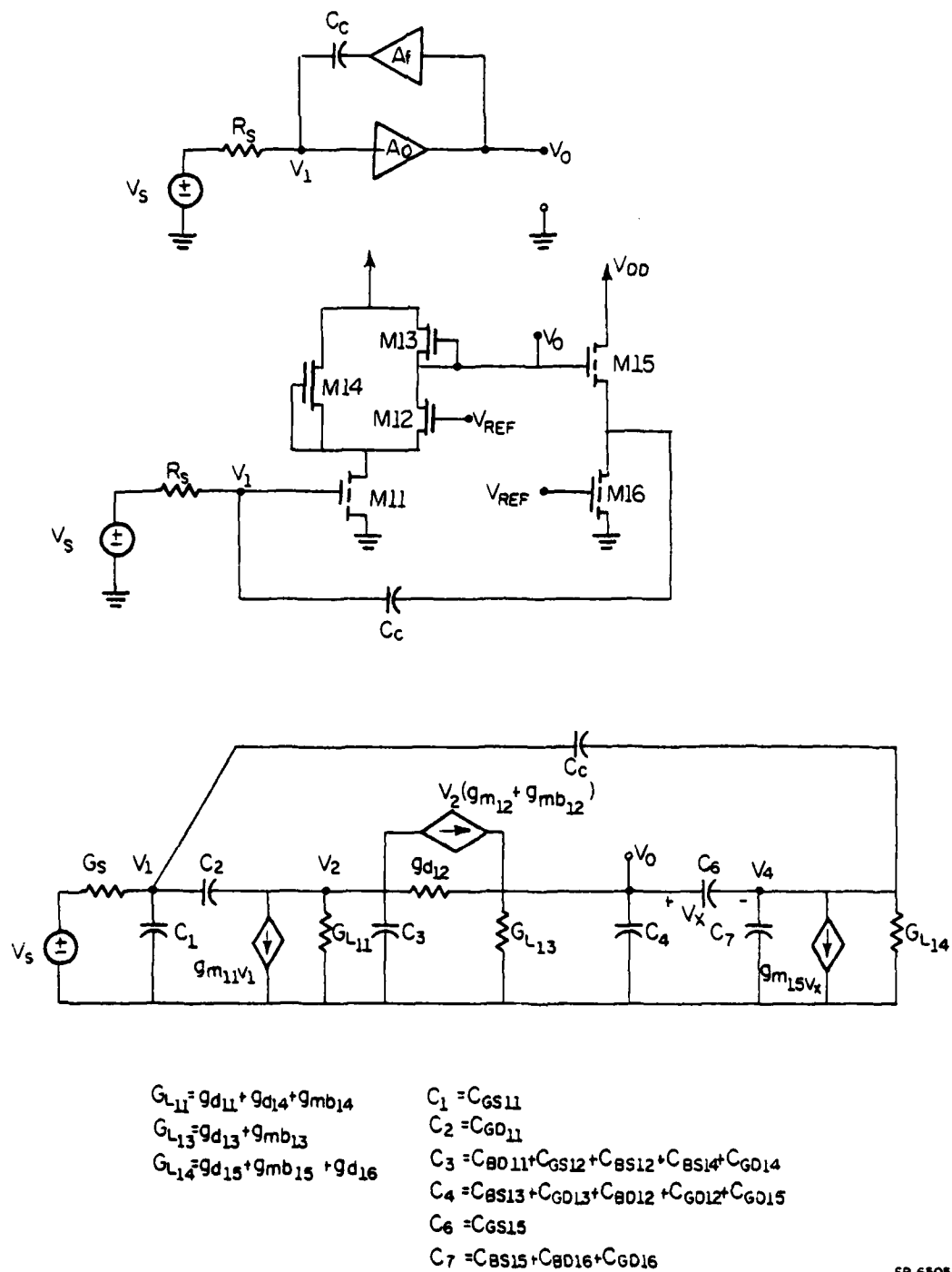
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Figure 5.7   Addition of a Buffer Amplifier in the Feedback Loop
a) Block Diagram   b) Circuit Implementation
c) Small Signal Circuit

which reveals the addition of another zero.

In general for a cubic equation with real roots one has,

$$(S + Z_1)(S + Z_2)(S + Z_3) = S^3 + (Z_1 + Z_2 + Z_3)S^2$$

$$+ (Z_1Z_2 + Z_1Z_3 + Z_2Z_3)S + Z_1Z_2Z_3$$

Dividing this expression through by the constant term gives,

$$S^3\left(\frac{1}{Z_1Z_2Z_3}\right) + S^2\left(\frac{1}{Z_2Z_3} + \frac{1}{Z_1Z_3} + \frac{1}{Z_1Z_2}\right) + S\left(\frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_3}\right) + 1$$

Therefore a small valued zero would lead to a dominant term in the S coefficient. Putting the expression for the numerator of V_o/V_s into this form the S coefficient is found to be,

$$S_{COEFFICIENT} = \left[\frac{C_2}{g_{m_{11}}} - \frac{(C_c + C_6 + C_7)}{(g_{m_{15}} + G_{L_{14}})}\right]$$

Since C_2 is the gate to drain capacitance of M11 it is much smaller than $(C_c + C_6 + C_7)$ while $g_{m_{11}}$ will generally be larger than $g_{m_{15}} + G_{L_{14}}$.

Inserting the values from Table 4.1 shows that the second term is 1069 times larger than the first leading to the approximation,

$$S_{COEFFICIENT} \simeq \left[-\frac{(C_c + C_6 + C_7)}{(g_{m_{15}} + G_{L_4})}\right]$$

Comparing this to the above general expression one is led to believe that $|Z_2| \gg |Z_1|$ and $|Z_3| \gg |Z_1|$ which gives

$$S_{COEFFICIENT} \simeq \frac{1}{Z_1} \quad \text{or} \quad Z_1 \simeq \frac{-(g_{m_{15}} + G_{L_{14}})}{(C_c + C_6 + C_7)}$$

Since one of the zero locations is known the remaining zeroes may be studied by factoring the known zero from the numerator expression. This may be accomplished by long division as shown in Figure 5.8 where it is

$$s + \dfrac{g_{m15}+G_{L14}}{C_c}$$

$$s^2 + s\left[\dfrac{g_{12}+G_{L11}}{C_2+C_3} + \dfrac{g_{12}C_2}{(C_2+C_3)C_6}\right] - \dfrac{g_{m11}g_{12}}{(C_2+C_3)C_6}$$

$$s^3 + s^2\left[\dfrac{g_{12}+G_{L11}}{C_2+C_3} + \dfrac{g_{12}C_2}{(C_2+C_3)C_6}\right] + s\left[\dfrac{g_{12}(g_{m15}+G_{L14})C_2}{(C_2+C_3)C_6C_c} - \dfrac{g_{m11}g_{12}}{(C_2+C_3)C_6}\right] - \dfrac{g_{m11}g_{12}(g_{m15}+G_{L14})}{(C_2+C_3)C_6C_c}$$

$$s^3 + s^2\left[\dfrac{g_{m15}+G_{L14}}{C_c}\right]\left[\dfrac{g_{12}+G_{L11}}{C_2+C_3} + \dfrac{g_{12}C_2}{(C_2+C_3)C_6}\right]$$

$$s^2\left[\dfrac{g_{12}+G_{L11}}{C_2+C_3} + \dfrac{g_{12}C_2}{(C_2+C_3)C_6}\right] + s\left[\dfrac{(g_{12}+G_{L11})(g_{m15}+G_{L14})}{(C_2+C_3)C_c} + \dfrac{g_{12}(g_{m15}+G_{L14})C_2}{(C_2+C_3)C_6C_c} - \dfrac{(g_{m15}+G_{L14})(g_{12}+G_{L11})}{C_c(C_2+C_3)}\right]$$

$$- s\,\dfrac{g_{m11}g_{12}}{(C_2+C_3)C_6}$$

$$- s\,\dfrac{g_{m11}g_{12}}{(C_2+C_3)C_6}$$

$$- \dfrac{g_{m11}g_{12}(g_{m15}+G_{L14})}{(C_2+C_3)C_6C_c}$$

$$0$$

Fig. 5.8 Numerator factorization

assumed that $C_c + C_6 + C_7 \simeq C_c$. Terms that have been crossed through are negligible for the range of values used.

The resulting quadratic, which defines the locations of the remaining two zeroes, should be compared to the previous numerator which was obtained before the buffer amplifier was added.

$$\text{WITH BUFFER AMP} \quad s^2 + s \left[\frac{g_{12} + G_{L_{11}}}{C_2 + C_3} + \frac{g_{12}C_2}{(C_2 + C_3)C_6} \right] - \frac{g_{m_{11}}g_{12}}{(C_2 + C_3)C_6}$$

$$\text{WITHOUT BUFFER AMP} \quad s^2 + s \left[\frac{g_{12} + G_{L_{11}}}{C_2 + C_3} + \frac{g_{12}C_2}{(C_2 + C_3)C_c} \right] - \frac{g_{m_{11}}g_{12}}{(C_2 + C_3)C_c}$$

The two expressions are seen to be identical except that C_c has been replaced by C_6. Since C_6 is smaller than C_c the RHP zero has been effectively moved to the right, out of the operating range of the amplifier. (Recall Figure 5.6 for decreasing values of C_c.) By substituting values from Table 4.1 into the numerator expression the zeroes are found to be,

$$z_1 = -12.2 \times 10^6 \quad z_2 = -743.7 \times 10^6 \quad z_3 = 489.1 \times 10^6$$

Therefore, the addition of capacitive feedback in conjunction with a buffer stage allows a dominant pole to be placed at $\omega_d = (R_s C_c A_o A_f)^{-1}$ while at the same time eliminating the ill effects produced by the RHP zero. In addition to this, a left half plane (LHP) zero at $\omega_z = (g_{m_{15}} + G_{L_{14}})/C_c$ may be placed to correspond with the first open loop pole of the cascode stage thereby extending the unity gain frequency of the amplifier. The value of this zero should be made to correspond to an open loop pole because it too could stop the 20 db per decade rolloff caused by the dominant pole if it occurs at too low a frequency. The ratio of ω_z to ω_d is given by,

$$\frac{\omega_z}{\omega_d} = R_s(g_{m_{15}} + G_{L_{14}})A_o A_f$$

If an amplifier has a low frequency gain of 60 db the buffer zero and the dominant pole should be separated by at least three decades in frequency to allow the gain to fall off as planned. This in turn places restrictions on R_s, $(g_{m_{15}} + G_{L_{14}})$ and $A_o A_f$ since the value of ω_z/ω_d should be at least 1000. Since R_s is very high in this design (due to the use of a depletion load in the differential stage) a practical value of $(g_{m_{15}} + G_{L_{14}})$ may be found.

The positions corresponding to poles other than the dominant pole are more difficult to pinpoint analytically. Their values depend a great deal on parasitic and gate capacitances. Therefore these capacitances should be minimized to obtain the largest open loop bandwidth possible.

The actual design of the compensation network proceeded as follows. The value of R_s was determined by the differential/level shift stage to be 287 kohms. Observing that the uncompensated 180 degree phase crossing occurred at 2.5 MHz and the low frequency gain was 61 db, the dominant pole frequency was chosen to be 1.7 kHz which would give the dominant pole the required 3 decades for sufficient gain rolloff. The value of A_f is 0.85 and in conjunction with the previously discussed cascode stage yields of value of 41.6 for the product $A_o A_f$. The required value of C_c was then calculated to be 8 pf.

It was next decided that the buffer zero should be placed at approximately 1.8 MHz which with the given value of C_c required that $(g_{m_{15}} + G_{L_{14}})$ have a value of 90 μmho. This is easily achieved by adjusting the current

through M16 and the gate to source voltage of M15. Note that the DC

voltage at the source of M15 is not critical because it doesn't serve as

a bias voltage for another stage.

The compensated frequency response of the amplifier is shown in

Figure 5.9. The dominant pole occurs at 1.7 kHz as expected and causes

the 20 db per decade rolloff from the DC gain of 61.8 db. Note also that

the 180 degree phase crossing has been extended from 2.5 MHz to 10 MHz by

the buffer zero. The resulting unity gain frequency is 3.16 MHz with a

corresponding phase margin of 85 degrees. These results meet the initial

design objectives.
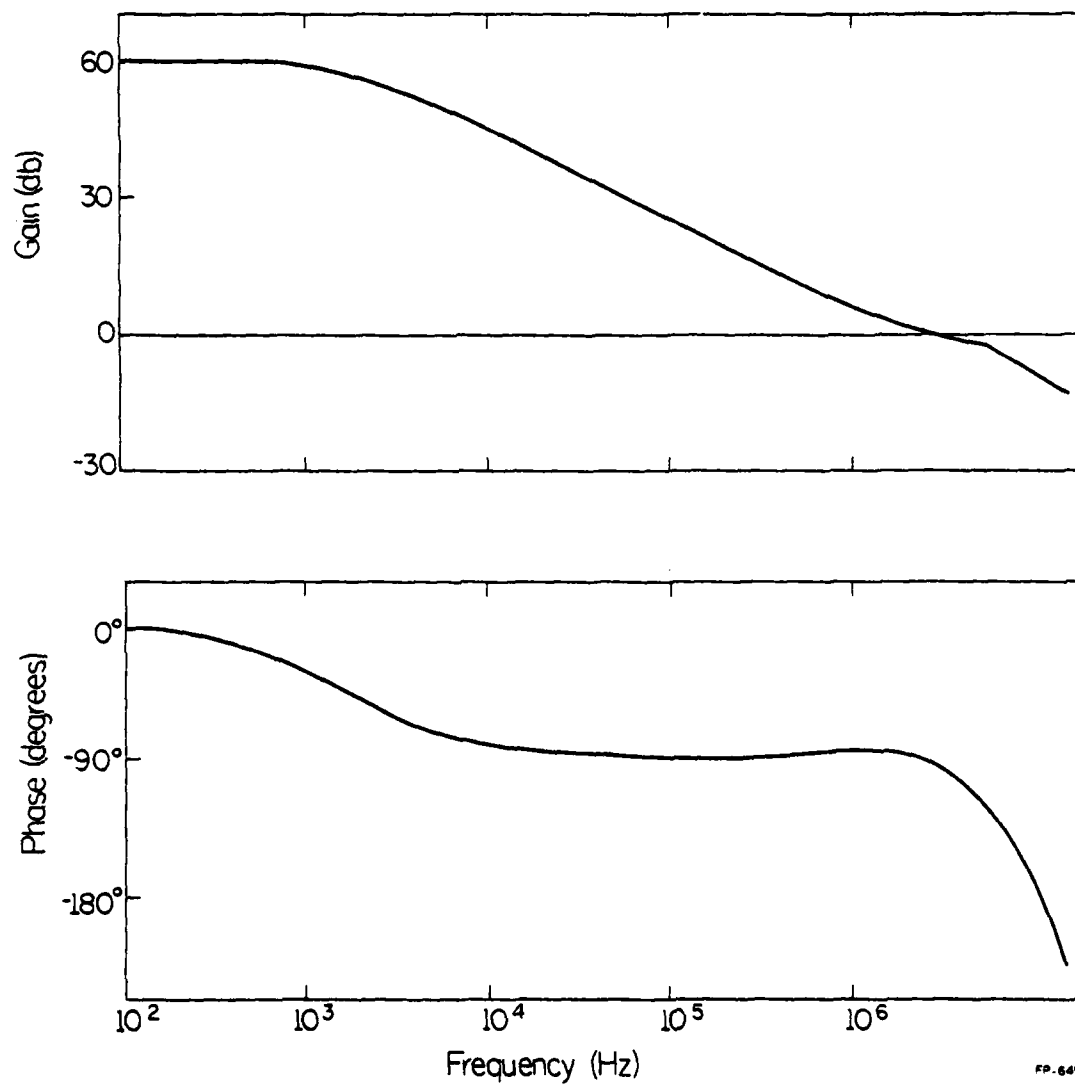
Figure 5.9   Compensated Frequency Response

6. Evaluation of Amplifier Performance

Several other performance criteria should be considered in addition
to the compensated frequency response. These include output voltage swing,
slew rate, driving capacitive loads and power consumption.

The output impedance must be low since a pole at $(R_{OUT} C_{LOAD})^{-1}$ is
created when driving capacitive loads. In order to not upset the frequency
compensation this pole should occur at a frequency greater than the unity
gain frequency of the amplifier. Figure 6.1 shows the amplifier's frequency
response when driving a 20 pF capacitive load. The unity gain frequency is
now 2.2 MHz with a phase margin of 51 degrees. A larger load capacitance
would degrade the frequency response further.

The value of C_c is an important factor with regard to slew rate as
well as chip area. Since the compensation capacitor is connected around
an inverting stage it must be charged and discharged by I9 and I16 respec-
tively under transient conditions. In order to obtain an acceptable slew
rate, without increasing I9 and I16 significantly, the compensation
capacitor should be as small as possible. Computer simulation yields a
slew rate of $\pm$ 2.2 volts/μ sec.

The quiescent DC power consumption is 16.3 mw. A trade off was made
between power consumption and output impedance as lower values of R_{OUT}
required large increases in I23 and I24.

The DC transfer curve of the amplifier, shown in Figure 6.2, reveals
a 5 volt p - p swing about the quiescent output voltage of 7.4 volts before
nonlinearities occur.

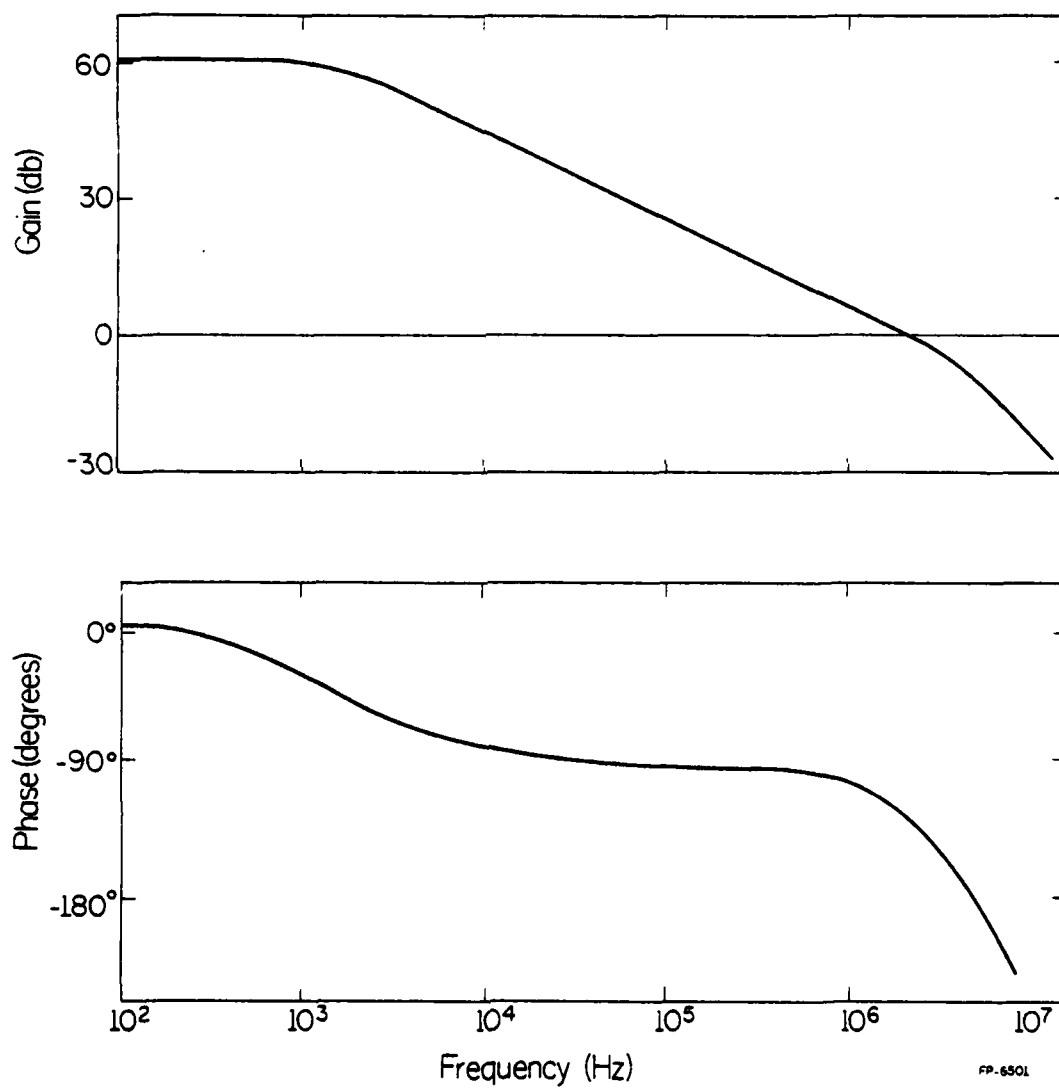A summary of amplifier performance is given in Table 6.1.

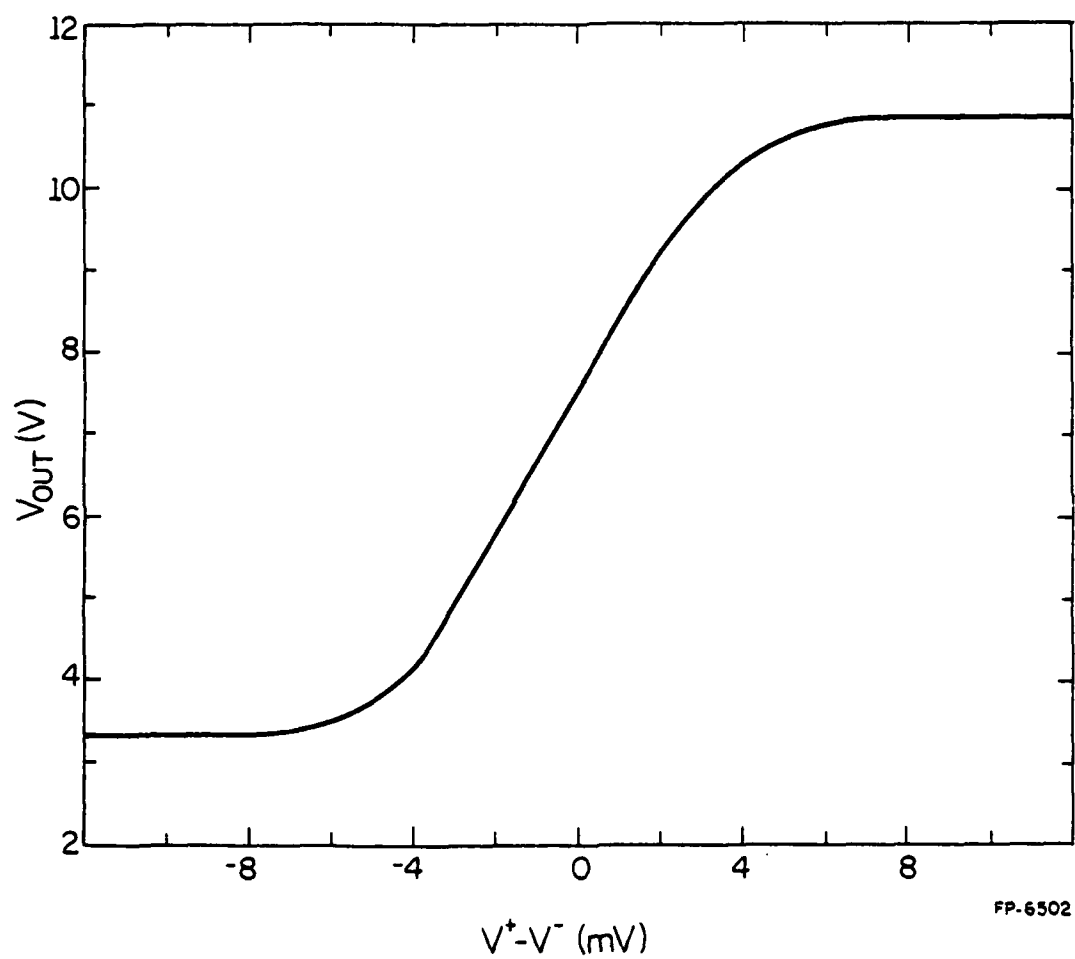Figure 6.1   Frequency Response With Capacitive Load

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Figure 6.2   DC Transfer Characteristic

Table 6.1 Amplifier Characteristics

Differential Open Loop Gain	61.8 db (1230)
Common Mode Gain	-0.5db (.94)
Common Mode Rejection Ratio	62.3db (1303)
Unity Gain Frequency	3.16 MHz
Phase Margin	85 degrees
180 degree Phase Shift Frequency	10 MHz
Gain Margin	8.8 db
Slew Rate	±2.2 volts/μ sec.
Input Impedance	10^{20} ohms
Output Impedance	2.87 kohms
Power Consumption	16.3 mw
C_c	8 pF
VDD	15 V
VSUB	-2.5

7. Summary

In this thesis the design of an NMOS operational amplifier with depletion loads has been proposed. Computer simulation using the SPICE circuit analysis program was used extensively in the design and analysis of the amplifier. Initial design goals were met indicating that circuits of this type can be expected to perform well. A detailed discussion of the method of frequency compensation revealed important design considerations with respect to individual device parameters.

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